

CLAIMS

We claim:

1. A method for processing a digital signal in multiple stages, the method comprising:

receiving a plurality of samples representing a digital signal, each sample represented electronically with a finite number of bits in a dynamic range; processing the samples through a series of coupled processing stages, wherein after at least one intermediate processing stage, the dynamic range of at least one of the samples is decreased without losing a significant bit; and passing the processed samples to an output interface.

2. The method of claim 1, wherein the dynamic range of at least one of the samples is decreased by:

selecting for the sample the smallest dynamic range in which the sample can be represented without losing a significant bit; and tracking the dynamic range for the sample.

3. The method of claim 1, wherein the dynamic range of at least one of the samples is decreased by:

selecting for the sample a dynamic range that is the larger of:

4 (1) the smallest dynamic range in which the sample can be represented
5 without losing a significant bit, and

6 (2) the largest dynamic range already selected for any other sample
7 between processing stages; and

8 tracking any dynamic range decrease for each output sample.

1 4. The method of claim 3, wherein tracking any dynamic range change includes
2 recording a change in dynamic range for each sample.

1 5. The method of claim 1, further comprising:
2 pre-processing the samples before processing the samples.

1 6. The method of claim 1, further comprising:
2 before each processing stage, normalizing the samples to be expressed in the same
3 dynamic range.

1 7. The method of claim 1, wherein each of the samples are represented
2 electronically with a different number of bits after a processing stage compared to before.

1 8. The method of claim 1, wherein the samples are represented in two's
2 complement binary notation.

1 9. A method for increasing the precision of a digital signal processed in multiple
2 consecutive stages, the method comprising:

3 reading a plurality of input samples, the input samples corresponding to an output
4 from a previous stage;
5 calculating a plurality of output samples using the input samples; and
6 for at least one output sample, decreasing the dynamic range of the output sample
7 if the output sample can be represented in a smaller dynamic range
8 without losing a significant bit.

1 10. The method of claim 9, wherein decreasing the dynamic range comprises
2 selecting the smallest dynamic range in which the output sample can be represented without
3 losing a significant bit.

1 11. The method of claim 9, wherein decreasing the dynamic range comprises:
2 selecting for each output sample a dynamic range that is the larger of:
3 (1) the smallest dynamic range in which the output sample can be
4 represented without losing a significant bit, and
5 (2) the largest dynamic range selected for any previously processed
6 output sample.

1 12. The method of claim 9, further comprising:
2 before calculating the output samples, normalizing the input samples to be
3 expressed in the same dynamic range.

1 13. The method of claim 9, further comprising:
2 storing the output samples in a memory for use in a next stage.

1 14. A method for increasing the precision of a digital signal processor, the method
2 comprising:

3 receiving a plurality of input samples representing a digital signal, each sample
4 represented electronically with a finite number of bits in a dynamic range;
5 calculating a plurality of output samples using the input samples;
6 decreasing the dynamic range of one or more of the output samples if an output
7 sample can be represented in a smaller dynamic range without losing a
8 significant bit; and
9 passing the processed digital communications signal to an output interface of the
10 digital signal processor.

1 15. The method of claim 14, wherein decreasing the dynamic range of each output
2 sample comprises:

3 selecting for an output sample the smallest dynamic range in which the output
4 sample can be represented without losing a significant bit; and
5 tracking the dynamic range for each output sample.

1 16. The method of claim 14, wherein decreasing the dynamic range of each output
2 sample comprises selecting for the output sample a dynamic range that is the larger of:

3 (1) the smallest dynamic range in which the output sample can be represented
4 without losing a significant bit, and
5 (2) the largest dynamic range selected for any previously processed output
6 sample.

1 17. The method of claim 14, wherein the output samples are represented in two's
2 complement binary notation.

1 18. A device for processing a digital signal in multiple stages, the device
2 comprising:

3 a calculation module adapted to compute a set of output samples using a set of
4 input samples; and

5 a post-calculation module operatively coupled to the calculation module, the post-
6 calculation module adapted to decrease the dynamic range of at least one
7 of the output samples for at least one stage if the output sample can be
8 represented in a smaller dynamic range without losing a significant bit.

1 19. The device of claim 18, wherein the calculation module is coupled to the post-
2 calculation module for receiving therefrom the output samples of a particular stage to use as
3 input samples of a next stage.

1 20. The device of claim 18, wherein the calculation module comprises a plurality
2 of calculation modules, each calculation module adapted to compute a set of output samples
3 using a set of input samples for one or more of the multiple stages.

1 21. The device of claim 18, wherein the post-calculation module is adapted to set
2 the dynamic range of each of the output samples, for a particular stage, to be the larger of:

- 3 (1) the smallest dynamic range in which the output sample can be represented
4 without losing a significant bit, and
5 (2) the largest dynamic range selected for a previously processed output sample in
6 the stage.

1 22. The device of claim 18, further comprising a pre-calculation module coupled
2 to the calculation module, the pre-calculation module adapted to normalize the dynamic
3 ranges of the input samples.

1 23. The device of claim 18, further comprising a final stage processor coupled to
2 the post-calculation module, the final stage processor adapted to normalize the dynamic
3 ranges of the output samples of a final stage.

1 24. The processor of claim 23, further comprising a dynamic range summer
2 coupled to the post-calculation module, the dynamic range summer adapted to calculate a
3 cumulative decrease in dynamic range over the multiple stages.

1 25. The processor of claim 23, wherein the final stage processor is adapted to
2 increase the dynamic ranges of the output samples of the final stage by a cumulative decrease
3 in dynamic range over the multiple stages.

1 26. A multi-stage digital signal processor comprising:
2 a calculation module adapted to compute a first set of output samples using a first
3 set of input samples;

4 a post-calculation module operatively coupled to the calculation module, the post-
5 calculation module adapted to decrease the dynamic range of at least one
6 of the first set of output samples if the first set output sample can be
7 represented in a smaller dynamic range without losing a significant bit;
8 and
9 a second calculation module coupled to the post-calculation module, the second
10 calculation module adapted to compute a second set of output samples
11 using a second set of input samples, the second set of input samples
12 corresponding to the first set of output samples.

1 27. A device for processing a digital signal in multiple stages, the device
2 comprising:
3 a plurality of stage modules operatively coupled together, the stage modules
4 adapted to process one or more stages, a stage module comprising:
5 a calculation module adapted to compute a set of output samples using
6 a set of input samples; and
7 a post-calculation module operatively coupled to the calculation
8 module, the post-calculation module adapted to decrease the
9 dynamic range of at least one of the output samples if the
10 output sample can be represented in a smaller dynamic range
11 without losing a significant bit;
12 wherein the set of output samples for a particular stage module is used for the set
13 of input samples for a next stage module.

1 28. The processor of claim 27, wherein at least two stage modules share a
2 calculation module.

1 29. A device for processing a digital signal in a series of consecutive stages in
2 which a set of output samples for one stage corresponds to a set of input samples for a
3 subsequent stage, the device comprising:
4 a storage means for storing the input and output samples of each stage;
5 a calculation means, for each stage, for computing a set of output samples using a
6 set of input samples; and
7 a postprocessing means for increasing the number of least significant bits retained
8 for an output sample without losing a significant bit.

1 30. The device of claim 29, wherein the postprocessing means comprises a means
2 for adjusting the dynamic range of an output sample.

1 31. A DSL modem comprising:
2 an input port for receiving a data signal;
3 a digital signal processor adapted to receive the data signal from the input port
4 and process the data signal in multiple stages, each stage resulting in a
5 plurality of output samples derived from a plurality of input samples,
6 wherein the digital signal processor is adapted to decrease the dynamic
7 range of one or more output samples of one or more stages without losing
8 a significant bit; and

an interface coupled to the digital signal processor for receiving therefrom a
processed data signal, the processed data signal corresponding to a
plurality of output samples from one of the stages.

32. The modem of claim 31, further comprising:
an analog front-end coupled to the interface, the analog front end adapted to
convert the data signal to an analog format for being transmitted over a
local loop.

33. The modem of claim 31, wherein the digital signal processor performs
discrete multi-tone modulation on the data signal in one or more of the stages.